In the Abstract:

Please delete the line at **page 12, line 5**, as follows:

~~Method for testing signals of an integrated circuit~~

Please delete the paragraph at **page 12, lines 7 to 9**, as follows:

~~In previously known methods for testing internal signals of an integrated circuit, additional output pins were required which, in general, were linked to additional measuring pads within the integrated circuit.~~

Please amend the paragraph at **page 12, lines 11 to 16**, as follows:

An integrated circuit can be tested externally without requiring additional testing output pins or test measuring pads. In the new method, the circuit functions are tested by using the output pins at which the output signal is present during normal operation of the integrated circuit. ~~By means of a simple, external connection with which a~~ A defined voltage value is applied to ~~set at~~ the signal output~~,~~ pin. An integrated control unit evaluates the applied voltage value, and in response thereto switches the integrated circuit ~~is switched by means of an integrated control unit~~ into a test mode in which it applies selected signals, which are to be tested, at the signal output pin. ~~There is no need for additional internal measuring pads or additional output pins.~~

REMARKS:

1) Referring to item 13) of the Office Action Summary, and section 1 on page 2 of the Office Action, relating to the Foreign Priority Claim, **the certified copy of the Foreign Priority Application has been filed by mail on April 15, 2003**, and was received in the USPTO Mailroom on April 21, 2003. The Examiner is respectfully requested to acknowledge receipt of the certified Priority Document, in the next official communication.

2) Referring to item 10) of the Office Action Summary, and section 2 on page 2 of the Office Action, the objection to the drawings has been addressed in the **enclosed Proposed Drawing Correction** with a cover letter directed to the Drawing Review Branch. Corrections have been marked in bold in Figs. 1 and 2, and a proposed new Fig. 3 is to be added to the application.

Regarding the "time windows" recited in original claim 5, note that original claim 5 has been canceled, and the new claims have avoided reciting such "time windows". Thus, the "time windows" do not need to be illustrated.

Regarding the two signal outputs recited in original claim 6, and in new claim 26, see the schematic illustration of the proposed new Fig. 3. The subject matter of Fig. 3 is supported by original claim 6 and the original description at page 3, lines 22 to 25, and thus does not introduce any new matter.

The other corrections in Figs. 1 and 2 merely bring the use of reference numbers and components of the drawing into

conformance with the written description. No new matter is involved.

Approval of the proposed corrections and the additional new Fig. 3 are respectfully requested. Also, the Examiner is respectfully requested to withdraw the objection to the drawings. Once the corrections are approved, proper corrected formal drawings will be filed.

3) Referring to section 3 on page 2 of the Office Action, the Examiner's attention is directed to the **additional Information Disclosure Statement that has been filed by mail on April 15, 2003** and received in the USPTO Mailroom on April 21, 2003. The Examiner is respectfully requested to consider the references, and to return an initialed, signed and dated acknowledgment copy of the corresponding Form PTO-1449 of April 15, 2003, together with next official communication.

4) The original specification, which was essentially a literal translation of a corresponding foreign text, has been amended in an editorial and formal manner to better comply with U. S. formal requirements and typical U. S. application style. A few features have also been clarified based on other portions of the written description and the disclosure of the original drawings. The "plural internal circuit blocks" now mentioned in the paragraph at page 5, lines 8 to 23 are originally disclosed at page 6, line 1, and page 7, line 33. The additional description of the new Fig. 3 that has been inserted near the end of page 8 is based on the original disclosure of claim 6 and page 3, lines 22 to 25 of

the specification. The present amendments are all supported by the substance and the context of the original disclosure, and do not introduce any new matter. Entry of the amendments is respectfully requested.

5) The prior claims have all been canceled. New claims 18 to 36 have been introduced. The new claims are based on the subject matter of the original claims and the other original disclosure, as shown in the following table, and do not introduce any new matter. Entry and consideration of the new claims are respectfully requested.

New Claims	18	19	20	21	22	23	24	25	26	27
Original Support	Cl.16; Figs. 1,2	Cl.17; Figs. 1,2	Figs. 1,2	Cl.1	Cl.2	Figs. 1,2	Cl.2	Cl.1; Figs. 1,2	Cl.6	Cl.3,4

New Claims	28	29	30	31	32	33	34	35	36
Original Support	Cl.8,9	Cl.8,9	Cl.5	Cl.5	Cl.5,10,11; Fig.2	Cl.7	Fig.2; Cl.5,7,10	Cl.10,11	Cl.12,13

6) The new claims 18 to 36 have been drafted "from the ground up" as a new or fresh approach to cover the inventive subject matter in a typical U. S. claim format and style. The claim construction of the new claims takes into account personal claim drafting style and preferences, as well as U. S. formal requirements.

7) Referring to sections 4 and 5 on page 3 of the Office Action, the objectionable terms in the original claims 1 to 13, 16 and 17 have been avoided in the preparation of the new claims. Accordingly, the Examiner is respectfully requested to withdraw the objection to the original claims, because this objection no longer applies.

8) Before particularly addressing the rejections of the original claims under 35 U.S.C. §112, the invention will first be discussed in general terms to provide a background.

The invention is generally directed to a circuit arrangement and a method that make it possible to test internal signal values generated in an integrated circuit, especially without requiring additional external test pins or measurement pads to be provided on the integrated circuit. Namely, the testing can be conducted through one or more of the already-existing normal signal output pins of the integrated circuit.

To achieve this, a voltage potential is established or applied to at least one of the ordinary signal output pins. The potential value of the externally applied voltage potential is evaluated, for example in a control unit within the integrated circuit. This evaluation, for example, involves comparing the externally applied potential value to one or more reference voltages or thresholds to determine whether the externally applied potential value lies in a particular range defined by the reference voltage or voltages.

Then, in response to and dependent on the result of the evaluation, the integrated circuit is switched from a normal

operating mode into a test mode. In the test mode, a test signal that is to be tested, rather than the normal output signal of the integrated circuit, is provided to the output signal pin, where it can be measured or tested.

Thus, the test mode can be initiated simply by externally applying or establishing a suitable voltage potential, i.e. a voltage potential with a proper potential value that will be evaluated to trigger the initiation of the test mode. Then, once the test mode has been initiated, the relevant test signal will appear at the output pin, so that it can be directly measured or tested at the output pin.

The structure of the circuit and the operation of the method are fully described in great detail in the original specification, also with reference to the drawings. As will be discussed with respect to particular aspects below, the invention now claimed is fully described in the specification so as to enable a person of ordinary skill in the art to practice the invention, and to reasonably convey to a person of ordinary skill that the present inventors had possession of the claimed invention at the time the application was filed.

9) The several claim rejections under 35 U.S.C. §112, first paragraph and second paragraph have been obviated by the cancellation of the original claims. Also, the issues raised in these rejections have been taken into consideration when preparing the new claims 18 to 36. The original claims were essentially a literal translation of corresponding foreign claims, and may have been somewhat difficult to follow in view

of the non-standard claim format, style and terminology. It is respectfully submitted that it will be more readily apparent that the invention as now defined in the new claims was clearly and fully disclosed in the original application disclosure. Namely, as will be discussed next, it is respectfully submitted that the invention as now more clearly defined in claims 18 to 36, is supported by a complete enabling disclosure which also demonstrates that the inventors had possession of the presently claimed invention when this application was filed.

10) Referring to section 7 on pages 3 to 5 of the Office Action, the rejection under 35 U.S.C. §112, first paragraph for lack of an enabling description is respectfully traversed.

The Examiner asserts that it is not clear from the specification "*what is switching the IC into a test mode*". Contrary to the Examiner's assertion, it is respectfully submitted that the original specification explains in clear and complete terms how the IC is switched into a test mode.

Generally, the actual "switching" into the test mode involves the control unit (ST) generating a control signal (MS, SE1, SE2), e.g. a logical "high" signal, that is provided to one of the two switching elements (E1 or E2), so as to connect the corresponding test signal output of the circuit unit (SCH) of the integrated circuit to the output pin (OUT) via the respective closed switch element (E1 or E2). **This is described in detail in the original specification at page 7, line 15 to page 8, line 9, or more generally at page 5, line 37 to page 6, line 10**. Thus, the "test mode" basically means that at least one of the

switching elements (E1, E2) is closed by the control signal (MS, SE1, SE2) that they have received, so that the corresponding test signal (SW1, SW2) to be tested is provided from the circuit unit (SCH) to the output pin (OUT). Moreover, the test mode can additionally involve the control unit suppressing the provision of the normal output signal to the output pin, and activating and deactivating different circuit blocks within the circuit unit.

The control unit (ST) is triggered or prompted to initiate the "test mode" as described above, by externally applying a proper voltage potential (e.g. a "test mode triggering potential" in a manner of speaking) to the output signal pin of the integrated circuit. The voltage potential that is applied to the output pin is evaluated by the control unit (ST), and the control unit will then issue the control signal (MS, SE1, SE2) to initiate the test mode in response to and dependent on the result of the evaluation of the externally applied voltage potential.

There are several ways in which the applied voltage potential may be evaluated, as described in the specification. Basically, the evaluation involves comparing the applied voltage potential to one or more reference voltages to determine whether the applied voltage potential lies in a specified voltage range for initiating the test mode. Preferably, this comparison can be carried out by means of one or more comparators (I1, I2, I3, I4), which compare the applied voltage potential to one or more reference voltages (V1, V2, V3, V4) to determine whether the applied voltage potential is at a level or in a range that has been specified (by setting the reference voltages) for triggering the test mode. Most preferably, at least two comparators form

a voltage window discriminator that determines whether the applied voltage potential lies within the range between an upper reference value and a lower reference value.

Furthermore, by providing at least two of such voltage window discriminators, the evaluation can determine not only whether the test mode shall be initiated, but also whether a first test signal or a second test signal should be provided to the output pin for testing. Still further, the evaluation can take into account the status of the normal output signal of the integrated circuit, by coupling the output signal value with the output values of the two comparators of a voltage window discriminator through a logic AND gate, so that the test mode is only triggered (i.e. the AND gate only gives a "true" signal) if the applied voltage potential lies in the pertinent range defined by the voltage window discriminator, and the output signal is zero. The above features are all described in the original specification at **page 3, lines 10 to 14 and 27 to 31; page 4, lines 5 to 12; page 6, line 15 to page 7, line 11 and page 7, line 25 to page 8, line 9.**

The Examiner has further asserted that it is not clearly described "*how the applicants determined the potential value and what is the potential value being used*". Contrary to the Examiner's assertion in this regard, the original specification clearly describes in detail how the externally applied potential value is established and how it is used. Namely, an external circuit arrangement, for example including two switches (T1, T2) respectively connected in series with two resistors (W1, W2) is connected to the output pin (OUT). By closing one of the

switches (e.g. T1), a current will be drawn from the internal voltage (VDD) through the load resistor (RL) and the node (50) and thus through the output pin (OUT), and then through the closed switch (T1) and the resistor (W1) to ground or some other reference voltage. Thus, the resulting voltage divider will establish a specified voltage potential value at the output pin (OUT). This voltage potential will, of course, exist at the internal node (50) to be tapped and evaluated by the control unit (ST) as described above. If a different voltage potential is to be applied to the output pin, then the switch (T1) can be opened and a different switch (T2) can be closed to connect a different-valued resistor (W2) to the output pin, thereby establishing a different output voltage. When both of the external switches are opened or disconnected, then the voltage at the node (50) and the output pin (OUT) will rise to the internal voltage (VDD).

In any event, the voltage existing at the output pin is evaluated by the control unit as discussed above. When the appropriate voltage potential for triggering the test mode is detected at the output pin, then the control unit will initiate the test mode as discussed above by generating and providing the switching control signal (MS, SE1, SE2) to the switching elements (E1, E2) and to the circuit unit (SCH). The designer or the user of the circuit can decide what particular potential values will be used to trigger the test mode (by correspondingly setting the reference voltage values V1, V2, V3, V4), based on considerations that are also fully described in the original specification. In this regard, see page 4, line 37 to page 5, line 6; page 5, lines

37 to 39; page 7, lines 25 to 39; also in connection with original Figs. 1 and 2.

Regarding "*how the potential value when applied to the OUT helps switched the IC into a test mode*", see the above discussion regarding how the comparators compare the externally applied voltage potential to the reference voltages (V1, V2, V3 and V4) to determine whether the externally applied potential is in the proper range for triggering the test mode, whereupon the logic gates (L1, L2) release the switching control signal (MS, SE1, SE2).

Regarding "*what is the voltage interval of the window*", and "*how these window discriminators help test the IC or even switch the IC to a test mode*", see the above discussion of how the window discriminators each comprise two comparators connected to upper and lower threshold reference voltages (V1 and V2 or V3 and V4) to determine whether the externally applied voltage potential lies in the range defined between these upper and lower reference voltages. Also see the above discussion of how the comparators, together with the AND gates (L1, L2) provide a logic signal as a control signal to the switching elements (E1, E2) so as to control the opening and closing of these switching elements, and thereby control the switching of the circuit into and out of the test mode.

In view of the above discussed portions of the original specification taken in connection with the drawings, it is respectfully submitted that a person of ordinary skill in the art upon reading the specification would be enabled to practice the present invention. A person of ordinary skill in the art is

readily familiar with the operation and circuit connection of commonly known circuit elements such as comparators, AND gates, resistors, switching elements, and the like. The operation of the circuit would already be understood even from the drawings, which also form a part of the original disclosure. For the above reasons, the Examiner is respectfully requested to withdraw the rejection under 35 U.S.C. §112, first paragraph for lack of an enabling disclosure.

11) Referring to section 8 on page 5 of the Office Action, the above discussion of the original disclosure also demonstrates that the original specification reasonably conveys that the inventors had possession of the presently claimed invention at the time this application was filed. For the above reasons, the Examiner is respectfully requested to withdraw the rejection under 35 U.S.C. §112, first paragraph for lack of an adequate written description demonstrating possession of the claimed invention.

12) Referring to section 10 on pages 6 to 7 of the Office Action, the new claims avoid the aspects found indefinite by the Examiner in the original claims. Accordingly, the new claims are not subject to the rejection under 35 U.S.C. §112, second paragraph, and the Examiner is respectfully requested to withdraw this rejection.

13) Referring to the "Conclusion" set forth at the middle of page 7 of the Office Action, with regard to the examination of the present claims in comparison to the prior art, it is respectfully submitted that the prior art neither discloses nor would have

suggested a method and a circuit arrangement by which an existing output pin of the integrated circuit is used "bi-directionally" and "multi-functionally" for normal signal output and for circuit testing, i.e. as a signal output pin for the output of a normal output signal during the normal operation of the IC, and as an input pin for applying a voltage potential to initiate a test mode, and further as a test output pin providing a test signal that is to be externally tested.

14) Favorable reconsideration and allowance of the application, including all present claims 18 to 36, are respectfully requested.

Respectfully submitted,

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Enclosures: Letter to Drawing Review Branch,
Hand-marked file copies of Figs. 1 and 2,
proposed new Fig. 3

CERTIFICATE OF FAX TRANSMISSION:

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_____ 6/17/03
Name: Walter F. Fasse - Date: June 17, 2003